ABSTRACT OF THE INVENTION

The memory device includes a memory cell array, and an output buffer receiving data addressed from the memory cell array and outputting the data based on a latency signal. A latency circuit selectively associates at least one transfer signal with at least one sampling signal based on CAS latency information to create a desired timing relationship between the associated sampling and transfer signals. The latency circuit stores read information in accordance with at least one of the sampling signals, and generates a latency signal based on the transfer signal associated with the sampling signal used in storing the read information.